Remarks:

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 8 - 17 are presently pending in the application. Claims 8, 10 and 14 have been amended. Claims 1 - 7 were previously canceled.

In item 5 of the above-identified Office Action, claims 8 – 10, 12 and 14 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 6,252,849 to Rom et al ("**ROM**") in view of U. S. Patent Application Publication No. 2004/0062200 to Kesavan ("**KESAVAN**"). In item 6 of the Office Action, claims 11, 13 and 15 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **ROM** and **KESAVAN**, in view of U. S. Patent Application Publication No. 2004/0151184 to Wang ("**WANG**"). In item 7 of the Office Action, claim 16 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **ROM** and **KESAVAN**, in view of U. S. Patent Application Publication No. 2004/0205228 to Rose ("**ROSE**") and U. S. Patent Application Publication No. 2003/0103521 to Raphaeli ("**RAPHAELI**"). In item 8 of the Office Action, claim 16 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **ROM** and **KESAVAN**, in view of **WANG**, **ROSE** and **RAPHAELI**.

Applicants respectfully traverse the above rejections.

More particularly, Applicants have amended independent claims 8 and 10 to even more clearly set forth that **the data packets that are counted by the packet counters are ingressed or egressed through each of the ports**, and that **the traffic volume is also controlled for each of the ports**. Support for these amendments can be found in the specification of the instant application, for example, in paragraphs [0013] and [0014] of the published application, which state:

> In accordance with an aspect of the present invention, an apparatus for controlling traffic over a network is provided, which comprises: a switching processor, including a plurality of ports connectable to a network line and packet counter registers for storing counting information on packets ingressed and egressed through the plurality of ports, **for controlling ingress and egress packet traffic volume for each of the plurality of ports** in response to an input traffic control command; **and a controller for registering, as a user value, traffic volume for each of the plurality of ports in an internal register**, the traffic volume being inputted through a data input unit, and for comparing a user value **for each of the plurality of ports** with a value in a respective one of the packet counter registers **for each port** so as to output the input traffic control command for each port to the switching processor. The input traffic control command may be a control command that enables the packets ingressed or egressed through each port to be queued, dropped, or paused.
>
> As described above, in accordance with the present invention, **traffic volume ingressed and egressed through each of the ports** of the switching processor can be adaptively controlled to be within an allowable range of traffic volume as preset by a control unit, so that the user can arbitrarily adjust traffic volume

> **for <u>each</u> port**, thereby achieving traffic volume control. [emphasis added by Applicants]

As such, the amendments to Applicants' independent claims 8 and 10 make it even more clear that **a plurality of ports are available, and that for <u>each</u> port, <u>an individual packet counter exists</u> that stores counting information for ingressing packets as well as egressing packets.**

As such, among other things, Applicants' claims require **an <u>individual</u> packet counter to be provided <u>for each port</u>.** This means that Applicants' particularly claimed device requires **an independent packet counter for <u>each</u> port.** See, for example, Applicants' amended claim 8, which recites, among other limitations:

> a controller for registering traffic volume for each of the ports in an internal register, said traffic volume being entered by a user through a data input unit as a user value, and **for comparing the user value for <u>each</u> of said plurality of ports with a value in a respective <u>one</u> of said packet counter registers for said <u>each</u> port** so as to output said input traffic control command for said each port to said switching processor. [emphasis added by Applicants]

Applicants' independent claim 10 recites similar limitations, among others. Additionally, Applicants' independent claim 14 recites, among other limitations:

> **comparing said user value with <u>a</u> respective value** for said traffic volume, said respective value being

written in a packet counter register; [emphasis added by Applicants]

As can be seen, Applicants' particularly claimed packet counter is arranged to monitor all data packets that are input or output through the respective port, meaning that the counter is always indicative of the traffic running through **a specific port.**

The foregoing limitations of Applicants' claims are neither taught, nor suggested by the prior art. More particularly, the **ROM** reference, cited on page 5 of the Office Action as allegedly showing a plurality of ports, does **not** disclose that a packet counter exists for each port that counts all packets ingressed and egressed through the specific port, as required by Applicants' claims. In fact, the **ROM** reference does not have any teaching or suggestion at all that data packets are output through the same ports as the packets are input. As can be seen from Fig. 3 of the **ROM** reference and col. 4 of **ROM**, lines 57 - 65, the switch of **ROM** uses counters that monitor the amount of data packets that are input through a specific port and that are, subsequently, forwarded into a buffer 305 of **ROM.** All data packets that are input through any of the plurality of ports are stored jointly in the buffer of **ROM.** Even though, in **ROM**, the counters are decremented when a data packet originating from their respective ports is output from

the common buffer, the counters of **ROM** do not represent the current traffic volume at each of the ports, as the buffers always induce a certain time delay. In fact, the counters of **ROM** merely provide an overview of the data packets that are going to be output from the specific port with which the buffer is associated. A current or dynamic overview over the actual data traffic at **all** individual ports – i.e., that are used for both **input and output** – is not taught or suggested by the **ROM** reference. According to the teaching of the **ROM** reference, a buffer for the data packets is inserted between the input at a first port and the output at a second port. As such, from this teaching of **ROM**, it is clear that the **ROM** reference does not disclose that packet counter registers are provided "for storing counting information on packets ingressed and egressed through each of the ports and for controlling ingress and egress packet traffic volume for each of the ports", as required by Applicants' independent claims 8 and 10.

Thus, the **ROM** reference does not teach that for each input/output port an individual counter is provided. The **KESAVAN** reference, cited in the Office Action in combination with the **ROM** reference, does not cure the foregoing deficiencies of the **ROM** reference.

More particularly, with regards to the **KESAVAN** reference, **KESAVAN** does not teach or suggest, among other limitations of Applicants' claims, that a control command is output to the switching processor. On page 2 of the Office Action, it is acknowledged that the **KESAVAN** reference only teaches a controller that issues commands such as dropping packets or allowing packets to pass to each port. Rather, pages 2 – 3 of the Office Action rely on **KESAVAN** for allegedly teachinbg the issuing of commands to a switching processor **in combination** with an alleged teaching in **ROM** of a switching processor that reacts to the received command. However, when combining the teachings of **KESAVAN** with those of **ROM**, in the manner suggested in the Office Action, it should be obvious – according to the arguments made in the Office Action – to where are these commands forwarded and how they are actually processed. Applicants respectfully submit that this seems to be an ex-post-evaluation of the documents, taking into account not only the teachings of **KESAVAN** and **ROM**, by themselves, but also the impermissible, hindsight use of the teachings of the present invention. Rather, absent such hindsight reconstruction, the **ROM** and **KESAVAN** references also fail to teach or suggest Applicants' particularly claimed feature of "a control command is output to the switching processor", among other limitations of Applicants' claims.

For the foregoing reasons, among others, Applicants' claims are believed to be patentable over the **ROM** and **KESAVAN** references. The **WANG**, **ROSE** and **RAPHAELI** references, cited in the Office Action in combination with **ROM** and **KESAVAN** against Applicants' dependent claims, do not cure the above-discussed deficiencies of the **ROM** and **KESAVAN** references.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 8, 10 and 14. Claims 8, 10 and 14 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 8, 10 or 14.

In view of the foregoing, reconsideration and allowance of claims 8 - 17 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

/Kerry Pauline Sisselman/
Kerry Pauline Sisselman
Reg. No. 37,237

For Applicants

July 26, 2010

Lerner Greenberg Stemer LLP
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101